US 20100006928A1

(19) United States

(12) Patent Application Publication

(10) Pub. No.: US 2010/0006928 A1

(43) Pub. Date: Jan. 14, 2010

Pan et al.

(54) STRUCTURE AND METHOD FOR FORMING A SHIELDED GATE TRENCH FET WITH AN INTER-ELECTRODE DIELECTRIC HAVING A LOW-K DIELECTRIC THEREIN

(76) Inventors: **James Pan**, West Jordan, UT (US); **James J. Murphy**, South Jordan, UT (US)

Correspondence Address:
TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER, EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834 (US)

(21) Appl. No.: **12/170,328**

(22) Filed: **Jul. 9, 2008**

Publication Classification

(51) **Int. Cl.**
H01L 29/00 (2006.01)
H01L 21/336 (2006.01)

(52) **U.S. Cl.** **257/330**; 438/272; 257/E29.001; 257/E21.409

(57) **ABSTRACT**

A shielded gate trench field effect transistor (FET) comprises trenches extending into a semiconductor region. A shield electrode is disposed in a bottom portion of each trench. The shield electrode is insulated from the semiconductor region by a shield dielectric. A gate electrode is disposed in each trench over the shield electrode, and an inter-electrode dielectric (IED) comprising a low-k dielectric extends between the shield electrode and the gate electrode.